WHAT IS CLAIMED:

1. An apparatus, comprising:

a microcontroller, said microcontroller comprising:

two data pointers, each data pointer pointing to a data memory location; and

a microcontroller core being capable of automatically incrementing/decrementing a selected one of the two data pointers based upon a value of an automatic increment/decrement (AID) enable bit and upon execution of a data pointer related instruction.

2. The apparatus of claim 1, wherein the data pointer related instruction is a data move instruction.

3. The apparatus of claim 1, wherein the microcontroller core is further capable of incrementing/decrementing the selected one of the two data pointers upon the execution of an increment instruction.

4. The apparatus of claim 1, wherein the microcontroller core automatically increments/decrements the selected one of the two data pointers when the AID enable bit is at a first logic value and does not automatically increment/decrement the selected one of the two data pointers when the AID enable bit is at a second logic value.

5. The apparatus of claim 1, wherein said microcontroller core further comprises an Arithmetic Logic Unit (ALU) wherein the automatic incrementing/decrementing instruction is performed.

6. The apparatus of claim 1, wherein said apparatus comprises at least one of: a microwave oven, a refrigerator, a television, a radio, a VCR, a stereos, a laser printer, a modem, a disk drive, an automotive engine controller, an automotive engine diagnosticator, and a climate controller.

7. In a microcontroller, a method for automatically incrementing/decrementing data pointers, said method comprising the steps of:

selecting a data pointer from two data pointers;

determining a value of a bit in a data pointer select register; and

automatically altering the value in the data pointer, based upon the value of the bit in the data pointer select register.

8. The method of claim 7, further comprising the step of:

determining whether an instruction is a data pointer related instruction, wherein the step of automatically altering the value in the data pointer is further based upon the determination that the instruction is a data pointer related instruction.

9. The method of claim 7, wherein the step of automatically altering the value in the data pointer comprises automatically incrementing the data pointer.

10. The method of claim 7, wherein the step of automatically altering the value in the data pointer comprises automatically decrementing the data pointer.

11. The method of claim 7, wherein the value in the data pointer is altered upon the value of the bit in the data pointer select register being at a first value and not altered upon the value of the bit in the data pointer select register being at a second value.

12. The method of claim 7, further comprising:

prior to the automatically altering step, executing a data pointer related instruction, wherein the step of automatically altering comprises the step of altering the value in the data pointer upon execution of the data pointer related instruction.

13. A microcontroller, comprising:

two data pointers;

a register, the register including at least a first bit and a second bit;

a selecting circuit for selecting one of the two data pointers based upon a value of the first bit of the register; and

a circuit for automatically altering the selected one of the two pointers based upon a value of the second bit of the register.

14. The microcontroller of claim 13, wherein the register is a data pointer select register within a special function register.

15. The microcontroller of claim 13, wherein the circuit comprises an adder/subtractor circuit for automatically incrementing/decrementing the selected one of the two data pointers based upon the value of the second bit of the register.

16. The microcontroller of claim 15, wherein the adder/subtractor circuit is configured to add one to or subtract one from the selected one of the two data pointers based upon at least a third bit of the register.

17. The microcontroller of claim 15, wherein said circuit further comprises an enabling circuit for enabling said adder/subtractor circuit following the execution of a data pointer related instruction by the microcontroller.

18. A method for operating a microcontroller in a processor-controlled apparatus, comprising the steps of:

first executing of a predetermined instruction, whereby the step of first executing does not cause a data pointer value to be modified based on a first value of a given indicator;

changing the given indicator to a second value;

second executing of the predetermined instruction, whereby the step of second executing does cause the data pointer value to be modified based on the second value of the given indicator.

19. The method of claim 18, wherein the given indicator comprises a bit in a register of the microcontroller and the data pointer value is modified in the step of second executing by at least one of incrementing and decrementing the data pointer value.

20. The method of claim 18, further comprising the steps of:

ascertaining that the given indicator comprises the first value; and

ascertaining that the given indicator comprises the second value.

21. The method of claim 18, wherein the predetermined instruction comprises a memory move instruction.

22. The method of claim 18, wherein the given indicator does not comprise the operand of the predetermined instruction.

23. An apparatus for automatically incrementing/decrementing a data pointer, comprising:

at least one data pointer;

at least one indicator; the at least one indicator capable of providing at least one of at least two values;

circuitry, the circuitry operably arranged with the at least one data pointer and the at least one indicator so as to enable the execution of a plurality of instructions; and

wherein the circuitry is configured such that execution of a specific instruction of the plurality of instructions results in the at least one data pointer being at least one of incremented and decremented when the at least one indicator comprises a first value of the at least two values and such that execution of the specific instruction of the plurality of instructions does not result in the at least one data pointer being either incremented or decremented when the at least one indicator comprises a second value of the at least two values.

24. The apparatus of claim 23, wherein the apparatus comprises a microcontroller.

25. The apparatus of claim 23, wherein the apparatus comprises an electronic device that includes at least one microcontroller.

26. The apparatus of claim 23, wherein the specific instruction comprises a memory move instruction.